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# Description

# [METHOD OF REDUCING PATTERN PITCH IN INTEGRATED CIRCUITS]

## BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention relates to a semiconductor fabrication process. More particularly, the present invention relates to a method of reducing pattern pitch.

[0003] Description of the Related Art

[0004] As the level of integration of integrated circuits continues to increase, the size of each semiconductor device and the distance between the devices in integrated circuits must be reduced. In other words, the minimum pattern pitch, the sum of pattern line-width and the space in an integrated circuit, must be as fine as possible. At present, the minimization of pattern pitch in integrated circuit fabrication is primarily driven by getting a finer photolithographic resolution. However, advances in photographic

resolution have become increasingly challenging and costly due to intrinsic optical limitations, increasingly challenging and costly due to intrinsic optical limitations. The 248-nm lithography, coupled with other resolution enhancement techniques, cannot be extended far beyond the 100-nm process technology node. The 193-nm lithography, cannot be extended far beyond the 70-nm technology node. The skyrocketing cost of photo-mask and resist for the 193-nm lithography further limits its wide applications. Further reduction in the minimum pitch in integrated circuits is thus more difficult after reaching certain photographic resolution limit. Without further reduction in pattern pitch, increasing the device packing-density and the level of integration of integrated circuits is virtually impossible. Alternative cost-effective approaches are desired.

## SUMMARY OF INVENTION

[0005] Accordingly, one objective of the present invention is to provide a method of reducing pattern pitch in integrated circuits.

[0006] A second objective of this invention is to provide a method of reducing pattern pitch in integrated circuits so that the device packing density in an integrated circuit can

be increased.

[0007] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of reducing pattern pitch. A material layer, a hard mask layer and a patterned photoresist layer are sequentially formed over a substrate. Using the patterned photoresist layer as etching mask, the hard mask layer is etched. Due to the trenching effect, a portion of the hard mask layer remains in an exposed region, which is not covered by photoresist and micro-trenches are formed at the edges of the exposed region. Thereafter, using the residual hard mask layer as etching mask, the material layer is patterned. Finally, the patterned photoresist layer and the hard mask layer are removed. In the invention, the trenching effect is utilized when etching the hard mask layer. A portion of the hard mask layer remains, and the micro-trenches are formed in the hard mask layer. The micro-trenches are transferred to the material layer subsequently in patterning the material layer, and the pattern pitch is made finer than the pitch of patterned photoresist layer.

[0008] This invention also provides a method of forming a pat-

terned mask for reducing pattern pitch. A mask layer is formed over a substrate. A patterned photoresist layer is formed over the mask layer. Thereafter, using the patterned photoresist layer as etching mask, the mask layer is etched. Utilizingthe trenching effect in plasma etching, a portion of the mask layer remains in an exposed region and micro-trenches are formed at the edges of the exposed region. The patterned photoresist layer is removed subsequently.

[0009] This invention also provides a method of reducing pattern pitch. A material layer is formed over a substrate. A patterned mask layer is formed on the material layer. Then, an etching process such as an ion reactive etching process using the patterned mask layer as etching mask is performed to form micro-trenches in the material layer, wherein the micro-trenches are formed in the material layer along the sidewalls of the patterned mask layer. The patterned mask layer is removed subsequently.

[0010] In this invention, the conventionally undesired trenching effect is utilized when etching the mask layer. As a result of the trenching effect, a portion of the mask layer remains within the exposed region, and micro-trenches are formed at the edges of the exposed region so that pattern

pitch can be reduced.

[0011] In this invention, the reactive ion etching process with specific recipes are utilized to etch the material layer. The reactive ions etch the material layer along sidewalls of the patterned mask layer to form micro-trenches in the material layer and reaching in the reduction of pattern pitch.

[0012] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

## BRIEF DESCRIPTION OF DRAWINGS

[0013] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0014] Figs. 1A to 1E are schematic cross-sections showing the steps in a manufacturing process capable of reducing pattern pitch according to one preferred embodiment of this invention.

[0015] Figs. 2A to 2C are schematic cross-sections showing the steps in a manufacturing process capable of reducing pat-

tern pitch according to another preferred embodiment of this invention.

## DETAILED DESCRIPTION

[0016] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0017] Figs. 1A to 1E are schematic cross-sections showing the steps in a manufacturing process capable of reducing pattern pitch according to one preferred embodiment of this invention. As shown in Fig. 1A, a material layer 102, a hard mask layer 104 and a patterned photoresist layer 108 are sequentially formed over a substrate 100. The material layer 102 is comprised of, for example, a conductive layer or an insulating layer or a dielectric layer. The hard mask layer 104 is formed, for example, by depositing a mask material over the material layer 102 to form a thin mask layer 105 and then depositing another mask material over the thin mask layer 105 to form a thick mask layer 107. A region exposed by the patterned photoresist layer is defined as an exposed region 120.

[0018] The etching selectivity of the hard mask layer 107 to the thin mask layer 105 needs be greater than 1. The etching selectivity of the material layer 102 to the thin mask layer 105 needs be as high as possible, for example, greater than 10. This is because the thick mask layer 107 will be etched first, and then the thin mask layer 105 will be patterned using the etched thick mask layer 107 as etching mask. Therefore, the etching selectivity of the hard mask layer 107 to the thin mask layer 105 should be greater than 1. In addition, if the etching selectivity of the material layer 102 to the thin mask layer 105 is high enough, the thin mask layer 105 can be made thinner and helps in better defining the material layer 102. In a preferred embodiment, the thin mask layer 105 is comprised of, for example, silicon oxide. The thick mask layer 107 is comprised of, for example, a silicon nitride layer.

[0019] Conventionally, the trenching effect is undesired while patterning the mask layer 104. Pattern pitch of the material layer is determined by the opening in the photoresist layer 108, and it is limited by the lithographic resolution limit. The conventional pattern pitch is $d_1$ which is a width of a line width and a space as shown in Fig. 1A. However, in the present invention, the trenching effect is utilized to

achieve the objective of the invention, as shown in Fig. 1B.

[0020] In Fig. 1B, using the patterned photoresist layer 108 as etching mask, the hard mask layer 104 is etched. Due to the trenching effect, a portion of the hard mask layer 104 remains in the exposed region 120, and micro-trenches 110 are formed at the edges of the exposed region 120. When the hard mask layer 104 consists of the thin mask layer 105 and the thick mask layer 107, the thick mask layer 107 is etched first. Because of the trenching effect, a portion of the thick mask layer 107 remains in the exposed region 120, and micro-trenches 110 are formed in the etched thick mask layer 107.

[0021] As shown in Fig. 1C, using the patterned photoresist layer 108 and the residual thick mask layer 107 as etching mask, the thin mask layer 105 is patterned to extend the two micro-trenches 110 into the thin mask layer 105 using a conventional plasma etch.

[0022] The width of the micro-trenches 110 can be controlled by regulating the etching chemistry. Alternatively, after forming the micro-trenches 110, an additional isotropic etching step can be conducted to regulate the width of the micro-trenches 110.

[0023] As shown in Fig. 1D, using the residual hard mask layer

104 as etching mask or using the residual photoresist layer 108 and the residual hard mask layer 104 as etching mask, the material layer 102 is patterned. Since the hard mask layer 104 has two micro-trenches 110, the two micro-trenches 110 also extend into the material layer 102. And the patterned material layer 102a is formed.

[0024] As shown in Fig. 1E, the patterned photoresist layer 108 and the hard mask layer 104 (shown in Fig. 1D) are removed to expose the patterned material layer 102a and a pattern having a pattern pitch $d_2$ of which is substantially smaller than that of $d_1$ the pitch of the patterned photoresist layer. The pattern pitch $d_2$ is about half of the pitch $d_1$ and the width of one space in the patterned photoresist layer 108 (as shown in Fig. 1A) is almost equal to the width of one line of the material layer 102a and two spaces in the material layer 102a. Hence, the method of present invention is capable of achieving a pattern pitch which is significantly finer than the pattern pitch of the patterned photoresist layer.

[0025] In summary, one major feature of this invention is that the trenching effect, conventionally undesired, is utilized for forming micro-trenches as substantially described above, and therefore manufacturing of a highly integrated device

can be realized.

[0026] Figs. 2A to 2C are schematic cross-sections showing the steps in a manufacturing process capable of reducing pattern pitch according to another preferred embodiment of this invention. As shown in Fig. 2A, a material layer 102 is formed over a substrate 100. The material layer 102 is comprised of, for example, a conductive layer or an insulating layer or a dielectric layer. A patterned mask layer 109 is formed on the material layer102, wherein the patterned mask layer is comprised of, for example, a photoresist layer or a layer with etching rate lower than the material layer 102. Especially, a pattern pitch d1 is the limitation of the lithographic process.

[0027] As shown in Fig. 2B, an etching process is performed using the patterned mask layer 109 as etch mask for forming micro-trenches 112 in the material layer 102, wherein the micro-trenches 112 are formed in the material layer 102 along the sidewalls of the patterned mask layer 109. In a preferred embodiment, the etching process is a reactive ion etching (RIE) process, and the pressure of the etching process is higher than 10 mTorrs. In addition, the bias power of the RIE process is lower than 150 W, and the source power of the RIE process is higher than 500W. The

reactive gas used in the RIE process comprises chlorine when the material layer 102 is a polysilicon layer and the patterned mask layer 109 is a silicon oxide layer.

[0028] As shown in Fig. 2C, the mask layer 109 is removed to expose the patterned material layer 102a with a pattern pitch d2, wherein the pattern pitch $d_2$ is about half of the pitch $d_1$ and the width of one space in the patterned photoresist layer 109 (as shown in Fig. 2A) is almost equal to the width of one line of the material layer 102a and two spaces in the material layer 102a. Therefore, the method of the present invention is capable of forming a pattern pitch, which is substantially smaller than the minimum pattern pitch which can be achieved by using the most advanced lithographic technology.

[0029] In this invention, the reactive ion etching process with specific recipes are utilized to etch the material layer. The reactive ions etch the material layer along sidewalls of the patterned mask layer to form the micro-trenches in the material layer. Therefore, the pattern pitch can be reduced and therefore the device packing density in integrated circuits can be effectively increased.

[0030] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure

of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.